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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,582	09/23/2003	**Alfred Stufflet**	1-2-0391.1US	2412

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EXAMINER	
MALEK, LEILA	
ART UNIT	**PAPER NUMBER**
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,582	STUFFLET ET AL.	
	Examiner	Art Unit	
	LEILA MALEK	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12,14-23 and 25-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9,10,12,14-18,20,21,23,25-32,34 and 35* is/are rejected.

7)☒ Claim(s) *8,11,19,22,33 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 02/02/2009 have been fully considered but they are not persuasive.

Applicant's Argument: Applicant argues on page 13, that Chein fails to teach a plurality of lookup tables.

Examiner's Response: in view of lack of any further details on the structure of the look-up tables in the claim, the examiner has given this limitation, its broadest reasonable interpretation. Therefore, buffer memory 135 and buffer memory 140 have been interpreted as look-up tables because they have the same functionality.

Applicant's Argument: Applicant argues on page 13, that the storage memory fails to teach how data values retrieved from the lookup tables may be used to generate processed data for controlling the digital module

Examiner's Response: Examiner asserts that Chien in column 4, lines 54-57, discloses that the data values retrieved from the lookup tables may be used to generate processed data (any control signal generated to control the digital module has been interpreted as processed data) for controlling the digital module (i.e. the DECT radio module).

Applicant's Argument: Applicant argues on page 14, that Pillekamp teaches away from including the registers within the radio port by using corresponding ports or registers located elsewhere.

Examiner's Response: Examiner respectfully disagrees. Examiner asserts that Pillekamp clearly teaches using a register in a burst mode controller (i.e. the radio interface unit 65, see the rejection of claim 23). Since reference Pillekamp does not discourage from using registers in radio ports, it does not teach away from this limitation.

Applicant's Argument: Applicant argues on page 14, that "the Examiner, citing Santos, alleges that it would have been obvious to one of skill in the art to use "memory-mapped" registers as they are the fastest registers. However, the Applicants respectively submit that the advantage gained in speed is also not disclosed by Santos."

Examiner's Response: Examiner respectfully asserts that reducing the data retrieval time from a memory is always desirable and by using a memory-mapped registers the time required to retrieve data would significantly decrease.

Applicant's Argument: Applicant argues on page 15, that "the look-up tables in Park fail to disclose the indexing scheme as disclosed in claims 1 and 12".

Examiner's Response: Examiner asserts that this limitation has been taught by Chien as explained above.

Applicant's Argument: Applicant argues on page 15, that "the look-up tables in Park fail to disclose the indexing scheme as disclosed in claim 1 and 12".

Examiner's Response: Examiner asserts that this limitation has been taught by Chien as explained above.

Applicant's Argument: Applicant argues on pages 15-16, that "Park fails to disclose using data values retrieved from the look-up table to generate processed data for controlling the digital module".

Examiner's Response: Examiner asserts that this limitation has been taught by Chien as explained above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 23, 26, 27, 31, 32, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien et al. (hereafter, referred as Chien) (US 6,308,062), in view of Pillekamp et al. (hereafter, referred as Pillekamp) (US 6,636,724).

As to claim 23, Chien shows a radio interface (see Fig. 2, blocks 65, 75, and 120) for interfacing between an analog radio module (see block 105, since analog module is part of the fixed radio module, it has been interpreted as analog radio module) and a digital module (see block 60), the interface comprising: a serial bus processor 120 (see column 4, lines 15-16), a programmable radio interface processor (RIP) 65 (see column 3, lines 38-40) coupled to the serial bus processor; and a plurality of lookup tables (see buffer memory 135 and buffer memory 140) indexed by data received from the analog radio module wherein data values retrieved from the lookup tables may be used to generate processed data for controlling the digital module (see column 4, lines 54-57). Chien discloses all the subject matters claimed in claim 23, except that the RIP (burst mode controller) includes at least one memory-mapped register. Pillekamp, in the same field of endeavor, discloses a mobile radio communication system comprising a DECT digital module (see column 1), and a burst mode controller (see column 2, lines 17-33). Pillekamp further discloses that raising or lowering of the transmission power in the radio part is initiated via corresponding ports or registers in a burst mode

controller (RIP). Since the Burst Mode controller is a control device, which controls the elements that are connected to it, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the Chien's radio interface device as suggested by Pillekamp and include the registers inside the radio interface device (or burst mode controller) in order to save the control information of the other units. Pillekamp is silent in disclosing that the registers are memory-mapped registers, however since the memory-mapped registers have the fastest mechanism for data retrieval (e.g. as evidence by Santos et al. (US 5,933,158. see column 24, first paragraph)), it would have been obvious to one of ordinary skill in the art at the time of invention to use these kind of registers instead of the registers suggested by Pillekamp.

As to claim 26, Chien discloses that serial bus processor 120 receives data from the plurality of lookup tables (see blocks 135 and 140), and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module (see column 4, lines 49-55).

As to claim 27, Chien shows that the burst mode controller is used to control the processed data generated by the serial bus processor 120 (see Fig. 2), therefore the combination of references used in rejection of claim 23, as explained above, meet all the limitations of claim 27.

As to claim 31, Chien does not expressly disclose a clock, coupled to the RIP, for determining relative timing of external events and for controlling the analog radio module. However, inherently every controller has a clock to accurately determine the time of external events of that processor, and for the same reason the analog radio

module should have a clock. Using only one clock to control the operation of the RIP and the analog signal would have been a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to use only one clock to reduce the cost of the circuit.

As to claim 32, Chien discloses that block 120 is a processor bus (p-bus) (see processor 140).

As to claim 34, Chien discloses that the burst mode controller accesses controlling software that is programmed according to one or more specific electronic characteristics of a given analog radio module (see column 3, lines 39-41, wherein radio architecture has been interpreted as e.g. the analog radio module).

3. Claims 1, 6, 7, 9, 10, 12, 18, 19, 20, 21, 25, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien and Pillekamp, further in view of Park et al. (hereafter, referred as Park) (US 6,373,902).

As to claims 1 and 12, Chien shows a radio interface (see Fig. 2, blocks 65, 75, and 120) for interfacing between an analog radio module (see block 105, since analog module is part of the fixed radio module, it has been interpreted as analog radio module) and a digital module (see block 60), the interface comprising: a serial bus processor 120 (see column 4, lines 15), a programmable radio interface processor (RIP) 65 (see column 3, lines 38-40) coupled to the serial bus processor; and a plurality of lookup tables (see buffer memory 135 and buffer memory 140) indexed by data received from the analog radio module wherein data values retrieved from the lookup tables may be used to generate processed data for controlling the digital module (see

column 4, lines 54-57). Chien further discloses that serial bus processor 120 receives data from the plurality of lookup tables (see blocks 135 and 140), and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module (see column 4, lines 49-55). Chien discloses all the subject matters claimed in claims 1 and 12, except that the RIP (burst mode controller) includes at least one memory-mapped register. Chien also does not disclose that the look-up tables are programmed with data so as to compensate for one or more non-linearlities which may be present n the analog radio module. Pillekamp, in the same field of endeavor, discloses a mobile radio communication system comprising a DECT digital module (see column 1), and a burst mode controller (see column 2, lines 17-33). Pillekamp further discloses that raising or lowering of the transmission power in the radio part is initiated via corresponding ports or registers in a burst mode controller (RIP). Since the Burst Mode controller is a control device, which controls the elements that are connected to it, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the Chien' radio interface unit as suggested by Pillekamp and include the registers inside the radio interface device (or burst mode controller) in order to save the control information of the other units. Pillekamp is silent in disclosing that the registers are memory-mapped registers, however since the memory-mapped registers have the fastest mechanism for data retrieval (e.g. as evidence by Santos et al. (US 5,933,158. see column 24, first paragraph)), it would have been obvious to one of ordinary skill in the art at the time of invention to use these kind of registers instead of the registers suggested by Pillekamp. Chien and Pillekamp disclose all the subject matters claimed in

claims 1 and 12, except that the lookup tables are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module, but are not accounted for in the digital module. Park discloses a device for linearizing a transmitter in a digital radio communication system (see the abstract). Park further discloses a plurality of lookup tables (see Fig. 3, blocks 351 and 353, and column 6, lines 5-9), which are indexed (as the I-channel pre-distortion look-up table and Q-channel pre-distortion lookup table) by data received from the analog radio module (see Fig. 3 and column 3, lines 50-57). Park further discloses that lookup tables are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module (see Figs. 2 and 3, wherein baseband filters 201 and 203 receive the outputs of look-up tables 351 and 353 to compensate for the non-linearties of the analog module (see also column 5, last paragraph) (the signal has been converted to analog before calculating the distortion, therefore the distortions are related to the analog signal). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Chien and Pillekamp as suggested by Park to compensate for the non-linearties of the analog signal (see the abstract) and as the result increase the performance of the system.

As to claims 6 and 17, Chien does not expressly disclose a clock, coupled to the RIP, for determining relative timing of external events and for controlling the analog radio module. However, inherently every controller has a clock to accurately determine the time of external events of that processor, and for the same reason the analog radio module should have a clock. Using only one clock to control the operation of the RIP

and the analog signal would have been a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to use only one clock to reduce the cost of the circuit.

As to claims 7 and 18, Chien discloses that block 120 is a processor bus (p-bus) (see processor 140).

As to claims 9 and 20, Chien discloses that the burst mode controller accesses controlling software that is programmed according to one or more specific electronic characteristics of a given analog radio module (see column 3, lines 39-41, wherein radio architecture has been interpreted as e.g. the analog radio module).

As to claims 10 and 21, Park further discloses that the nonlinearities include at least one of AGC (automatic gain control) line voltage as a function of gain, and power level control voltage as a function of power output (see Fig. 3, blocks 217 and 223, and column 6, lines 49-51), whereby the digital module need not be modified to work with the specific characteristics of a given analog radio module (i.e. the analog signal nonlinearities have been compensate before the transmission of signal to the digital module (see Figs. 5 and 6). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Chien and Pillekamp as suggested by Park to compensate for the non-linearties of the analog signal (see the abstract) and as the result increase the performance of the system.

As to claim 25, Chien and Pillekamp disclose all the subject matters claimed in claim 23, except that the lookup tables are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module. Park

discloses a device for linearizing a transmitter in a digital radio communication system (See the abstract). Park further discloses a plurality of lookup tables (See Fig. 3, blocks 351 and 353, and column 6, lines 5-9), which are indexed (as the I-channel pre-distortion look-up table and Q-channel pre-distortion lookup table) by data received from the analog radio module (see Fig. 3 and column 3, lines 50-57). Park further discloses that lookup tables are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module (see Figs. 2 and 3, wherein baseband filters 201 and 203 receive the outputs of look-up tables 351 and 353 to compensate for the non-linearties of the analog module (see also column 5, last paragraph) (the signal has been converted to analog before calculating the distortion, therefore the distortions are related to the analog signal). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Chien and Pillekamp as suggested by Park to compensate for the non-linearties of the analog signal (see the abstract) and as the result increase the performance of the system.

As to claim 35, Chien and Pillekamp disclose all the subject matters claimed in claim 23, except that the non-linearlities include at least one of AGC line voltage as a function of gain, and power level control voltage as a function of power output. Park discloses that the nonlinearities include at least one of AGC (automatic gain control) line voltage as a function of gain, and power level control voltage as a function of power output (see Fig. 3, blocks 217 and 223, and column 6, lines 49-51), whereby the digital module need not be modified to work with the specific characteristics of a given analog radio module (i.e. the analog signal nonlinearities have been compensate before the

transmission of signal to the digital module (see Figs. 5 and 6). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Chien and Pillekamp as suggested by Park to compensate for the non-linearties of the analog signal (see the abstract) and as the result increase the performance of the system.

4. Claims 28 and 29 rejected under 35 U.S.C. 103(a) as being unpatentable over Chien and Pillekamp, further in view of Fischer et al. (hereafter, referred as Fischer) (US 5,768,695).

As to claim 28, Chien and Pillekamp disclose all the subject matters claimed in claim 23, except that the radio interface unit includes a finite state machine equipped to access registers. Fischer, in the same field of endeavor, discloses an apparatus for providing a flexible interface for creating the necessary control signaling of a radio transmitter (see column 1, first paragraph). Fischer, further discloses a radio interface unit 402 (see Fig. 3), which includes a register set 406, which is coupled to the state machine 404 (see column 4, lines 27-39). It would have been obvious to one of ordinary skill in the art at the time of invention to use a radio interface unit as suggested by Fischer including a state machine having access to the register sets to provide the appropriate signals to the other parts of the system (see column 5, lines 4-6).

As to claim 29, Fischer further discloses that the radio interface 402 includes a processor interface (the state machine 404 has been interpreted as processor interface) for accessing the register. It would have been obvious to one of ordinary skill in the art at the time of invention to use a radio interface unit as suggested by Fischer including a

state machine (or processor interface) having access to the register sets to provide the appropriate signals to the other parts of the system (see column 5, lines 4-6).

5. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chien, Pillekamp, and Fischer, further in view of Bhandal et al. (hereafter, referred as Bhandal) (US 6,532,533).

As to claim 30 Chien, Pillekamp, and Fischer, disclose all the subject matters claimed in claim 28 except that the radio interface includes one or more GPIO registers for accessing the memory-mapped registers. Bhandal discloses a processing device which provides general-purpose input/output pins for use by software routines as needed (see the abstract). Bhandal further discloses that GPIO pins are driven or monitored by reading or writing to a set of memory mapped registers (see column 4, lines 27-34). It would have been obvious to one of ordinary skill in the art at the time of invention to use the method taught by Bhandal to simplify the system (see column 2, lines 25-35).

6. Claims 3, 4, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien, Pillekamp, park, further in view of Fischer.

As to claims 3, 4, 14, and 15, Chien, Pillekamp, and park disclose all the subject matters claimed in claims 1 and 12, except that the radio interface unit includes a finite state machine equipped to access registers. Fischer, in the same field of endeavor, discloses an apparatus for providing a flexible interface for creating the necessary control signaling of a radio transmitter (see column 1, first paragraph). Fischer further discloses a radio interface unit 402 (see Fig. 3), which includes a register set 406,

which is coupled to the state machine 404 (see column 4, lines 27-39). It would have been obvious to one of ordinary skill in the art at the time of invention to use a radio interface unit as suggested by Fischer including a state machine having access to the register sets to provide the appropriate signals to the other parts of the system (see column 5, lines 4-6). In view of lack of any description for processor interface, the processor interface has been interpreted as the state machine.

7. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien, Pillekamp, park, and Fischer, further in view of Bhandal et al. (hereafter, referred as Bhandal) (US 6,532,533).

As to claims 5 and 16 Chien, Pillekamp, park, and Fischer, disclose all the subject matters claimed in claims 3 and 14 except that the radio interface includes one or more GPIO registers for accessing the memory-mapped registers. Bhandal discloses a processing device which provides general-purpose input/output pins for use by software routines as needed (see the abstract). Bhandal further discloses that GPIO pins are driven or monitored by reading or writing to a set of memory mapped registers (see column 4, lines 27-34). It would have been obvious to one of ordinary skill in the art at the time of invention to use the method taught by Bhandal to simplify the system (see column 2, lines 25-35).

Allowable Subject Matter

8. Claims 8, 11, 19, 22, 33, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEILA MALEK whose telephone number is (571)272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
Art Unit 2611

/L. M./
/Leila Malek/
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